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TFT LCD Approval Specification

MODEL NO.: N156B3
Suffix:-L0B

Customer : Acer

Approved by :

Note :

核准時間	部門	審核	角色	投票
2010-06-01 14:05:51	NB 產品管理處	楊 2010.06.01 竣 傑	Director	Accept

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 3.0	Feb.02, 2010	All	All	Approval spec is first issued
Ver. 3.1	Feb.22, 2010	15	5.4	Update EDID code content
				Preliminary spec, pixel clock:69.3MHz
				Approval spec, pixel clock:75.46MHz
Ver.3.2	May.27, 2010	25	9	Update package drawing

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156B3-L0B is a 15.6" (15.547" diagonal) TFT Liquid Crystal Display module with CCFL Backlight unit and 30 pins LVDS interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 FEATURES

- HD (1366 x 768 pixels) resolution
- 3.3V LVDS (Low Voltage Differential Signaling) interface
- CCFL

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	344.232 (H) x 193.536 (V) (15.547" diagonal)	mm	(1)
Bezel Opening Area	349.58 (H) x 198.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.252 (H) x 0.252 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	358.8	359.3	359.8	mm	(1)
	Vertical(V)	209	209.5	210	mm	
	Thickness(T)	-	5.9	6.2	mm	
Glass Thickness		0.45	0.5	0.55	mm	
		0.45	0.5	0.55	mm	
Weight		---	465	480	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

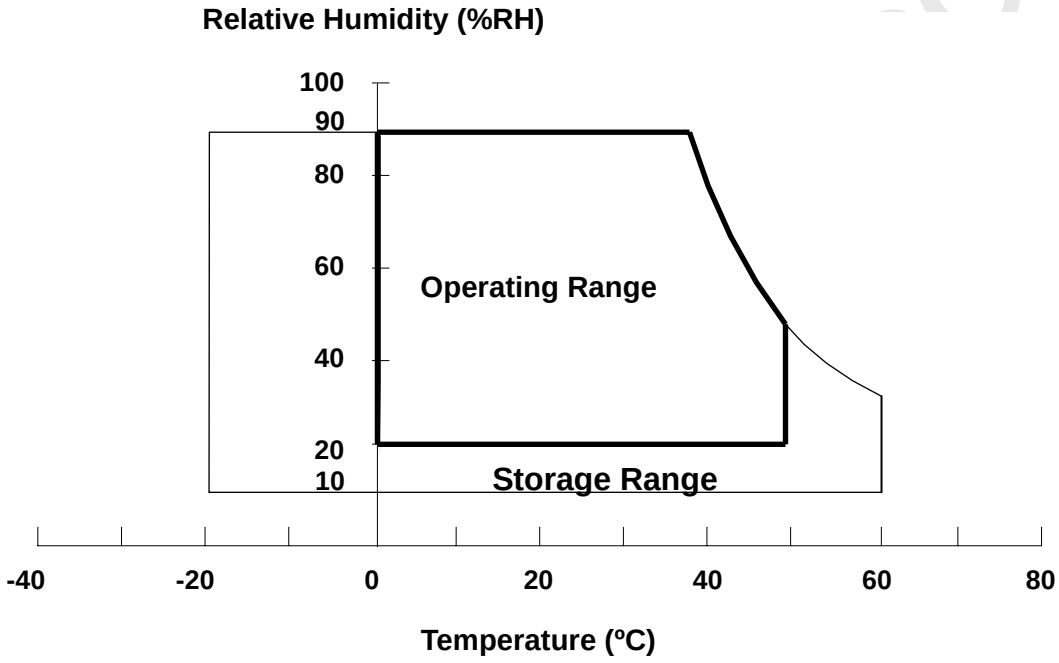
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.

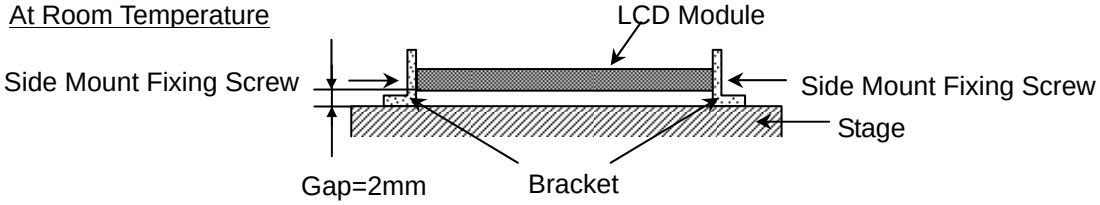


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10~500 Hz, 0.5hr/cycle 1cycle for X,Y,Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	--	720	V_{RMS}	(1), (2), I_L = 6.0 mA
Lamp Current	I_L	--	6	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	40	60	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

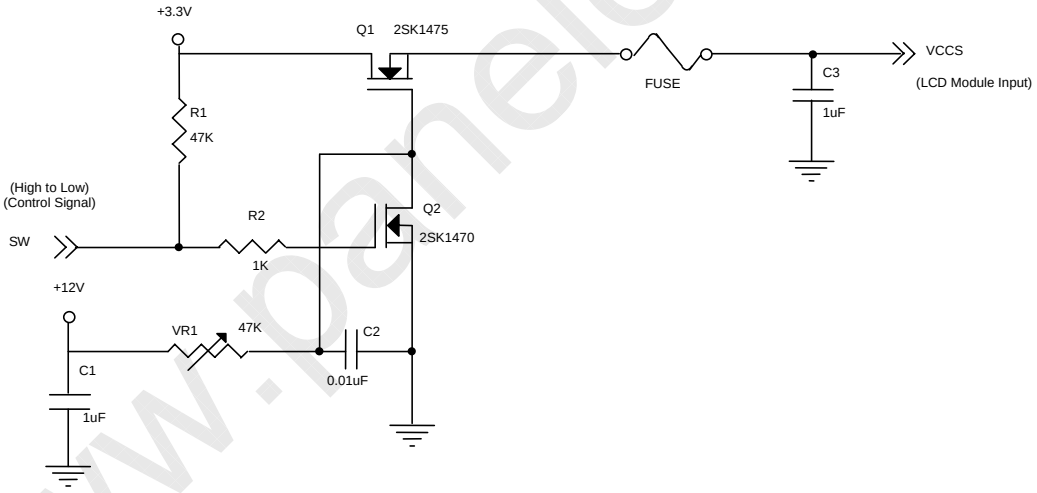
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	-
Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	-	210	240	mA	(3)a
	Black		-	320	350	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(4), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(4) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(4)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(4)
LVDS Terminating Resistor		R_T	-	100	-	Ohm	-
Power per EBL WG		PEBL	-	2.9	-	W	(5)

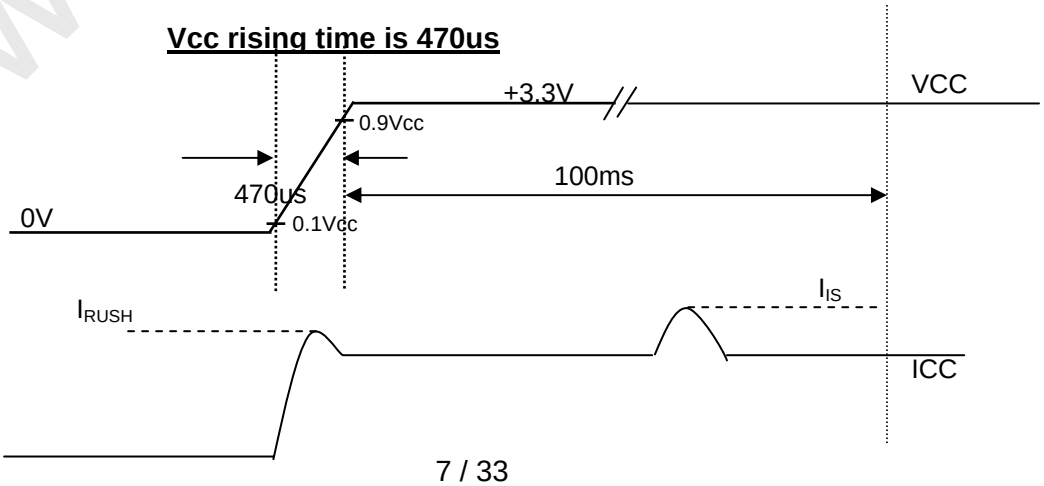
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.





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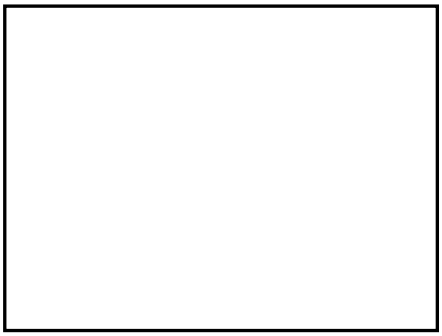
Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

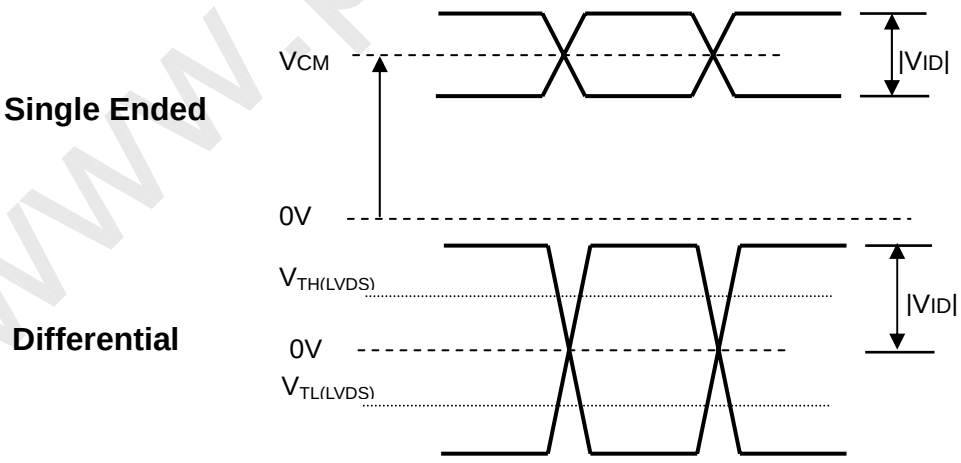
(a) Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

(d) The inverter used is provided from Sumida.. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.



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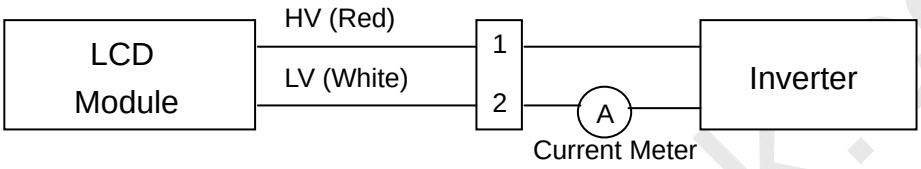
3.2 BACKLIGHT UNIT Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	648	720	792	V_{RMS}	I_L = 6.0 mA
Lamp Current	I_L	2.0	6.0	7.0	mA_{RMS}	(1),(2)
		3.0				(1),(3)
Lamp Turn On Voltage	V_S	--	--	1300(25 °C)	V_{RMS}	(4)
		--	--	1560(0 °C)	V_{RMS}	(4)
Operating Frequency	F_L	40	--	60	KHz	(5)
Lamp Life Time	L_{BL}	15,000	--	--	Hrs	(7)
Power Consumption	P_L	--	4.32	--	W	(6), I_L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) for burst mode inverter design

Note (3) for continuous mode inverter design

Note (4) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise, the lamp may not be turned on normally.

Note (5) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (6) $P_L = I_L \times V_L$

Note (7) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 6.0 mA_{RMS} until one of the following events occurs:

(a) When the brightness becomes ≦ 50% of its original value.

(b) When the effective ignition length becomes ≦ 80% of its original value. (The effective ignition length is a scope that luminance is over 70% of that at the center point.)

Note (8) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the

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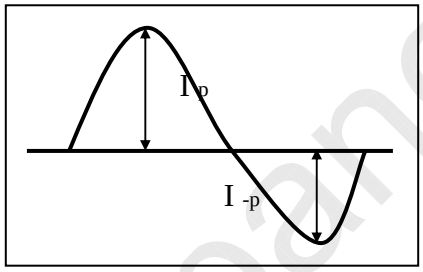
inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;
b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
c. The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{rms}

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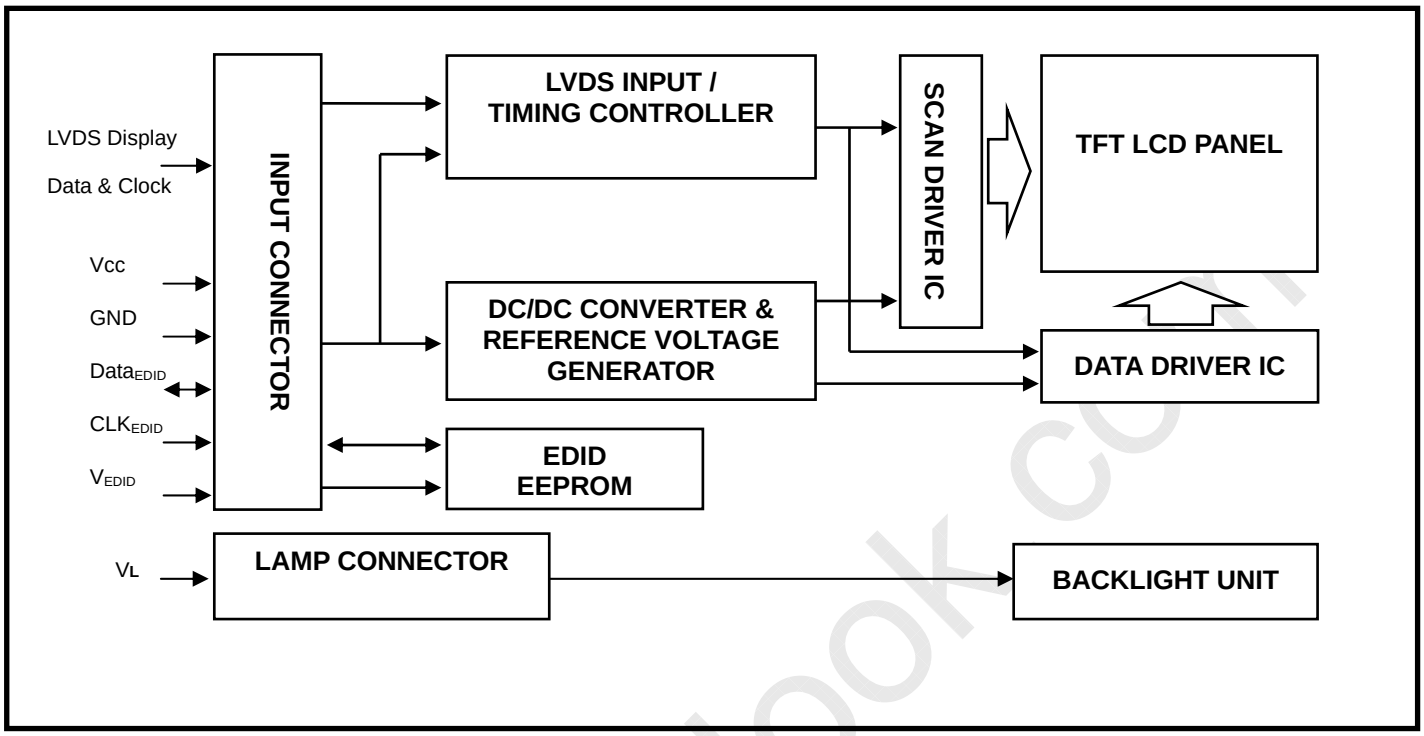
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	VCCS	Power Supply (3.3V typ.)		
3	VCCS	Power Supply (3.3V typ.)		
4	VEDID	DDC 3.3V power		
5	TEST	Panel Self Test		
6	CLKEDID	DDC clock		
7	DATAEDID	DDC data		
8	Rxin0-	LVDS differential data input	Negative	R0-R5, G0
9	Rxin0+	LVDS differential data input	Positive	
10	VSS	Ground		
11	Rxin1-	LVDS differential data input	Negative	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	Positive	
13	VSS	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	Positive	
16	VSS	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	CE	Color Engine Enable Input		
20	NC	No Connection (Reserve)		
21	NC	No Connection (Reserve)		
22	VSS	Ground		
23	NC	No Connection (Reserve)		
24	NC	No Connection (Reserve)		
25	VSS	Ground		
26	NC	No Connection (Reserve)		
27	NC	No Connection (Reserve)		
28	VSS	Ground		
29	NC	No Connection (Reserve)		
30	NC	No Connection (Reserve)		

Note (1) Connector Part No. : JAE FI-XB30SRL-HF11,P-TWO-187106-30091、Starconn-093F30-B0T11A or equivalent

Note (2) User's connector Part No: JAE - FI-X30H or equivalent,

Note (3) The first pixel is odd as shown in the following figure.

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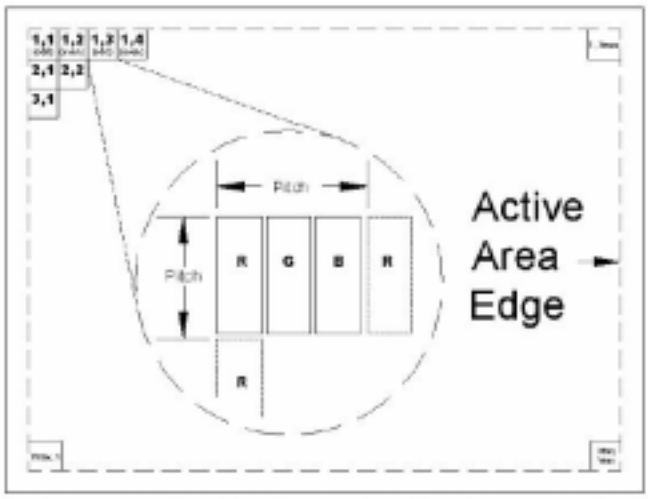
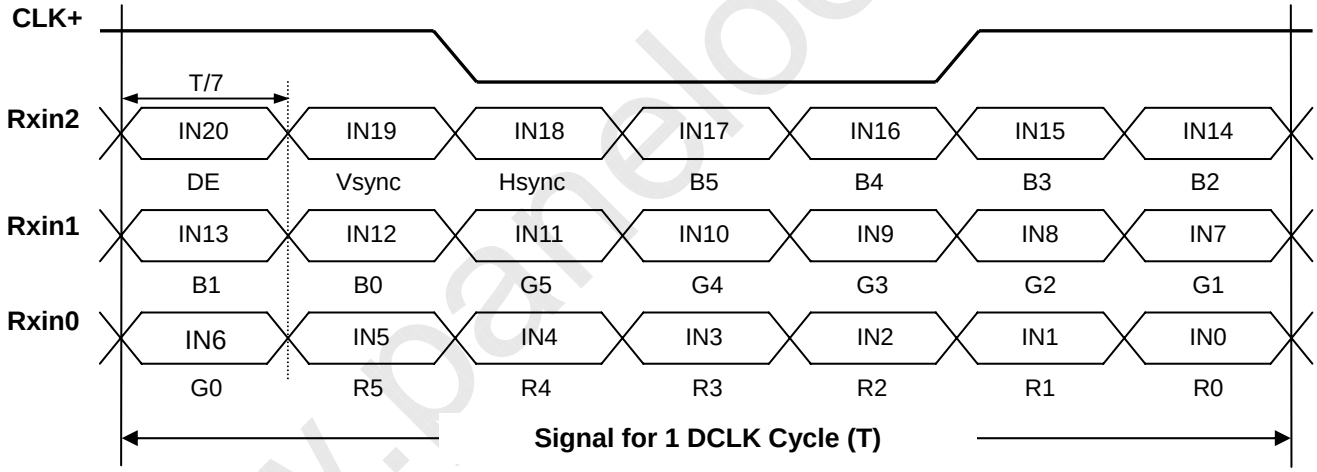


5.2 TIMING DIAGRAM OF LVDS INPUT SIGNAL



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5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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5.4 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N156B3-L0B)	99	10011001
11	0B	ID product code (hex LSB first; N156B3-L0B)	15	00010101
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	07	00000111
17	11	Year of manufacture (fixed year code)	14	00010100
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Max H image size (“34.42cm”)	22	00100010
22	16	Max V image size (“19.35cm”)	13	00010011
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	3D	00111101
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	95	10010101
27	1B	Rx=0.578	94	10010100
28	1C	Ry=0.339	56	01010110
29	1D	Gx=0.312	4F	01001111
30	1E	Gy=0.556	8E	10001110
31	1F	Bx=0.158	28	00101000
32	20	By=0.149	26	00100110
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001

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41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“75.46MHz”, According to VESA CVT Rev1.1)	7A	01111010
55	37	# 1 Pixel clock (hex LSB first)	1D	00011101
56	38	# 1 H active (“1366”)	56	01010110
57	39	# 1 H blank (“210”)	D2	11010010
58	3A	# 1 H active : H blank (“1366 : 210”)	50	01010000
59	3B	# 1 V active (”768”)	00	00000000
60	3C	# 1 V blank (”30”)	1E	00011110
61	3D	# 1 V active : V blank (”768 :30”)	30	00110000
62	3E	# 1 H sync offset (”60”)	3C	00111100
63	3F	# 1 H sync pulse width (" 40”)	28	00101000
64	40	# 1 V sync offset : V sync pulse width (”3 : 6 ”)	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”60 : 40 : 3 : 6 ”)	00	00000000
66	42	# 1 H image size (”344 mm”)	58	01011000
67	43	# 1 V image size (”193 mm”)	C1	11000001
68	44	# 1 H image size : V image size (”344 : 193”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name “N156B3-L0B”, ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name (“N”)	4E	01001110
78	4E	# 2 2nd character of name (“1”)	31	00110001
79	4F	# 2 3rd character of name (“5”)	35	00110101
80	50	# 2 4th character of name (“6”)	36	00110110
81	51	# 2 5th character of name (“B”)	42	01000010
82	52	# 2 6th character of name (“3”)	33	00110011
83	53	# 2 7th character of name (“-”)	2D	00101101
84	54	# 2 8th character of name (“L”)	4C	01001100
85	55	# 2 9th character of name (“0”)	30	00110000

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86	56	# 2 9th character of name (“B”)	42	01000010
87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with “Blank” character	20	00100000
89	59	# 2 Padding with “Blank” character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor “CMO”, ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string (“C”)	43	01000011
96	60	# 3 2nd character of string (“M”)	4D	01001101
97	61	# 3 3rd character of string (“O”)	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with “Blank” character	20	00100000
100	64	# 3 Padding with “Blank” character	20	00100000
101	65	# 3 Padding with “Blank” character	20	00100000
102	66	# 3 Padding with “Blank” character	20	00100000
103	67	# 3 Padding with “Blank” character	20	00100000
104	68	# 3 Padding with “Blank” character	20	00100000
105	69	# 3 Padding with “Blank” character	20	00100000
106	6A	# 3 Padding with “Blank” character	20	00100000
107	6B	# 3 Padding with “Blank” character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N156B3-L0B”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“N”)	4E	01001110
114	72	# 4 2nd character of name (“1”)	31	00110001
115	73	# 4 3rd character of name (“5”)	35	00110101
116	74	# 4 4th character of name (“6”)	36	00110110
117	75	# 4 5th character of name (“B”)	42	01000010
118	76	# 4 6th character of name (“3”)	33	00110011
119	77	# 4 7th character of name (“-”)	2D	00101101
120	78	# 4 8th character of name (“L”)	4C	01001100
121	79	# 4 9th character of name (“0”)	30	00110000
122	7A	# 4 9th character of name (“B”)	42	01000010
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with “Blank” character	20	00100000
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	48	01001000

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6. INTERFACE TIMING

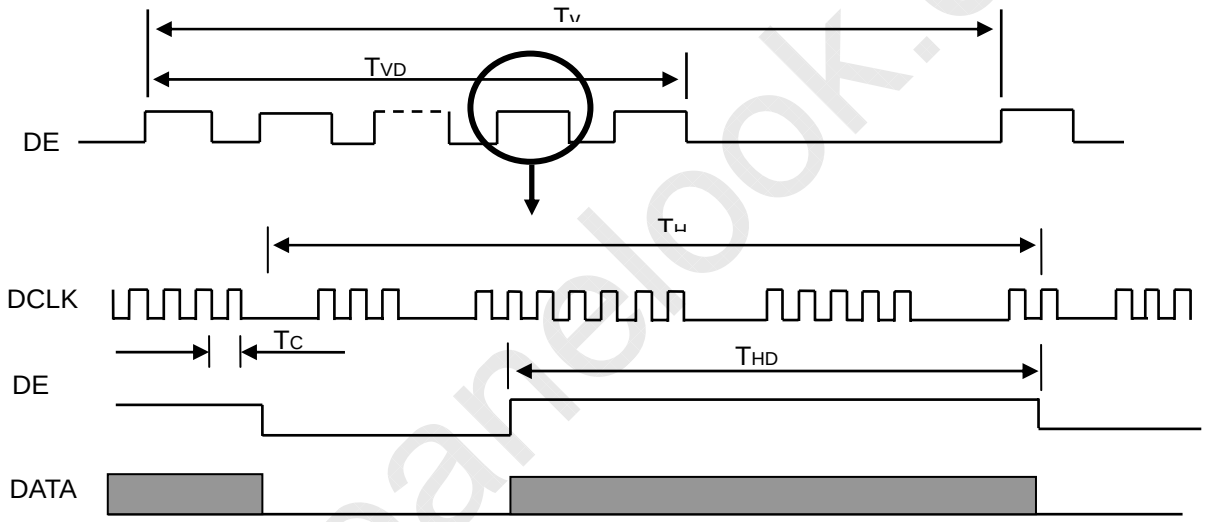
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	67.91	75.46	79.23	MHz	-
DE	Vertical Total Time	TV	773	798	806	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	30	TV-TVD	TH	-
	Horizontal Total Time	TH	1412	1576	1628	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	210	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM



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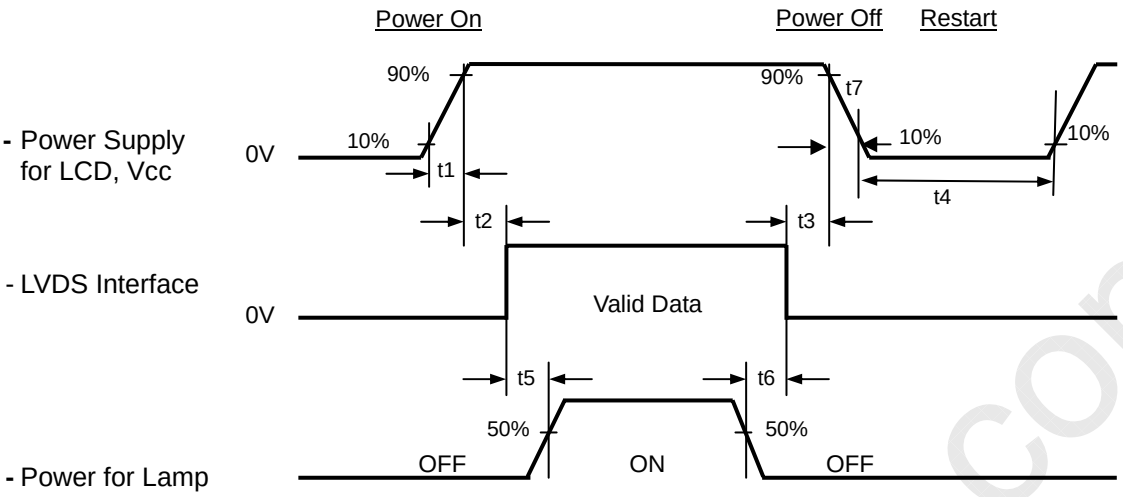
6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 ≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 50μs≦t7≦300 ms.

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7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
CCFL Input Current	I_L	6	mA

The measurement methods of optical characteristics are shown in Section 8.2. The following items should be measured under the test conditions described in Section 8.1 and stable environment shown in Note (5).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	350	500	--	NA	(2), (5) (7)
Response Time		T_R		--	3	8	ms	(3) (7)
		T_F		--	7	12	ms	
Average Luminance of White		L_{AVE}		170	200	--	cd/m^2	(4), (6) (7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.578	Typ + 0.03	NA	(1) (7)
		Ry			0.339		NA	
	Green	Gx			0.312		NA	
		Gy			0.556		NA	
	Blue	Bx			0.158		NA	
		By			0.149		NA	
	White	Wx			0.313		NA	
		Wy			0.329		NA	
Viewing Angle	Horizontal	θ_x+	CR≥10	40	45	--	Deg.	(1),(5) (7)
		θ_x-		40	45	--		
	Vertical	θ_Y+		15	20	--		
		θ_Y-		40	45	--		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	90	--	%	(5),(6) (7)

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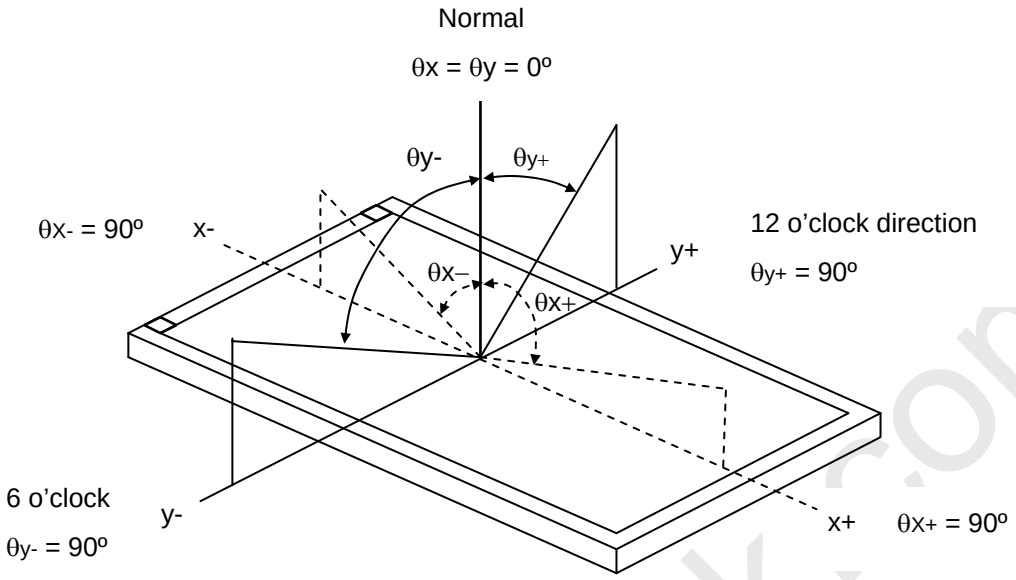
Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

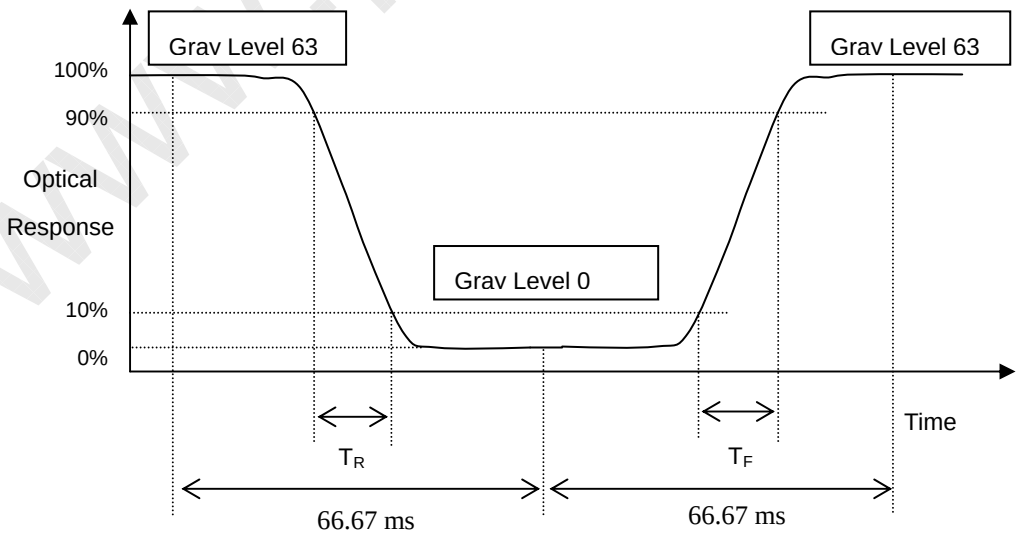
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



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Note (4) Definition of Average Luminance of White (L_{AVE}):

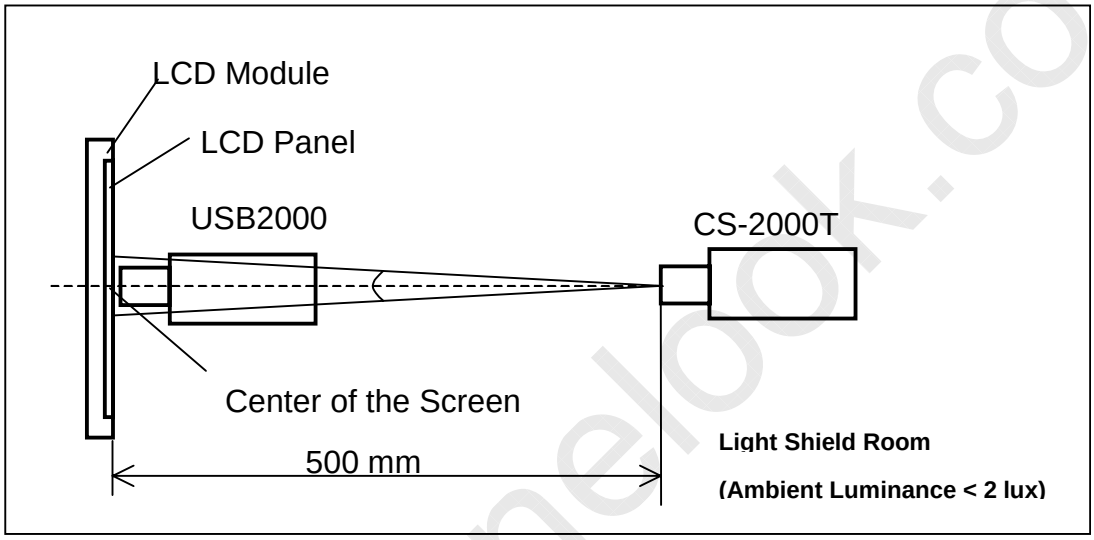
Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%

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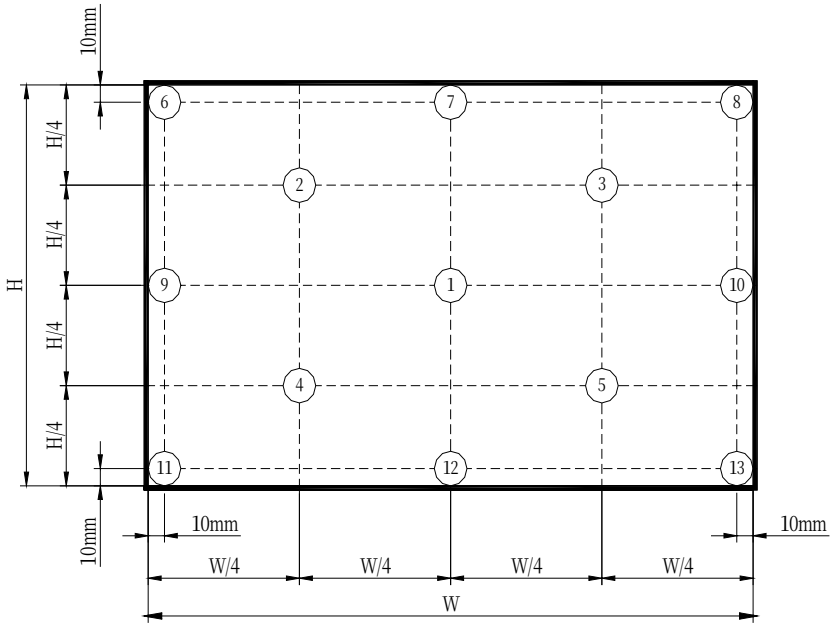

Ⓧ : Test Point

X=1 to 13

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

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9. PACKING

9.1 CARTON

(1) Box Dimensions : 442(L)*392(W)*300(H)
(2) 20 modules/Carton

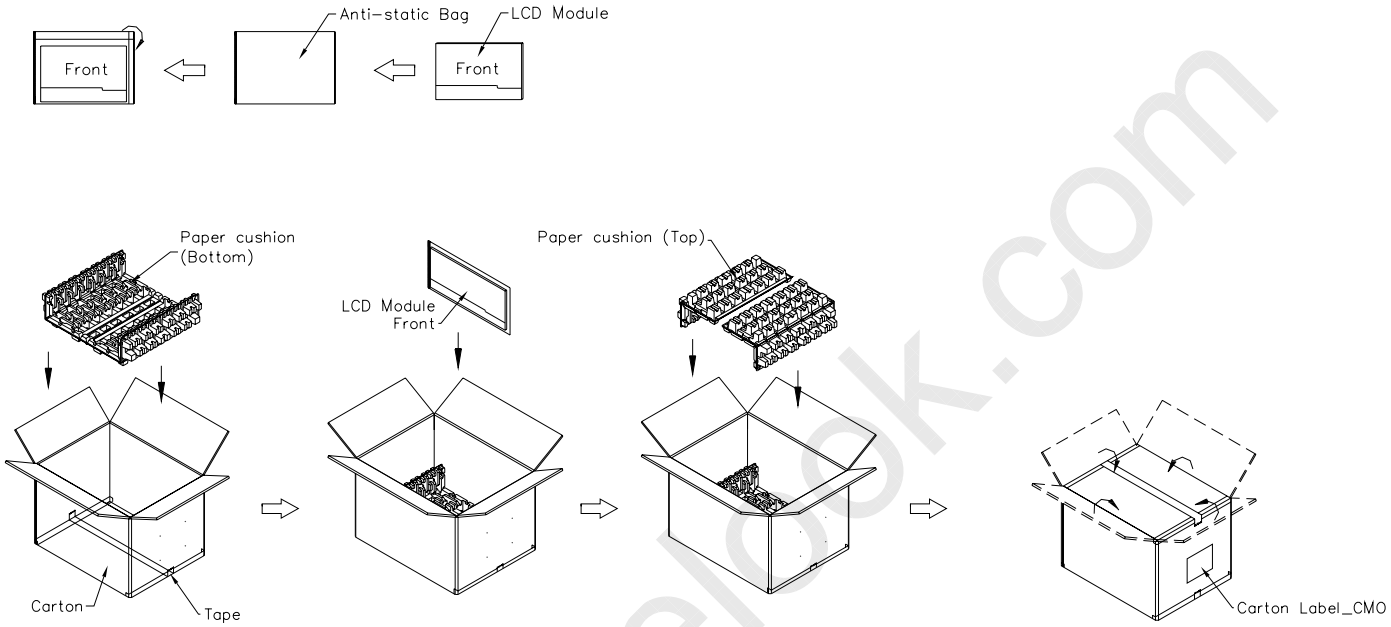

Figure. 9-1 Packing method

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9.2 PALLET

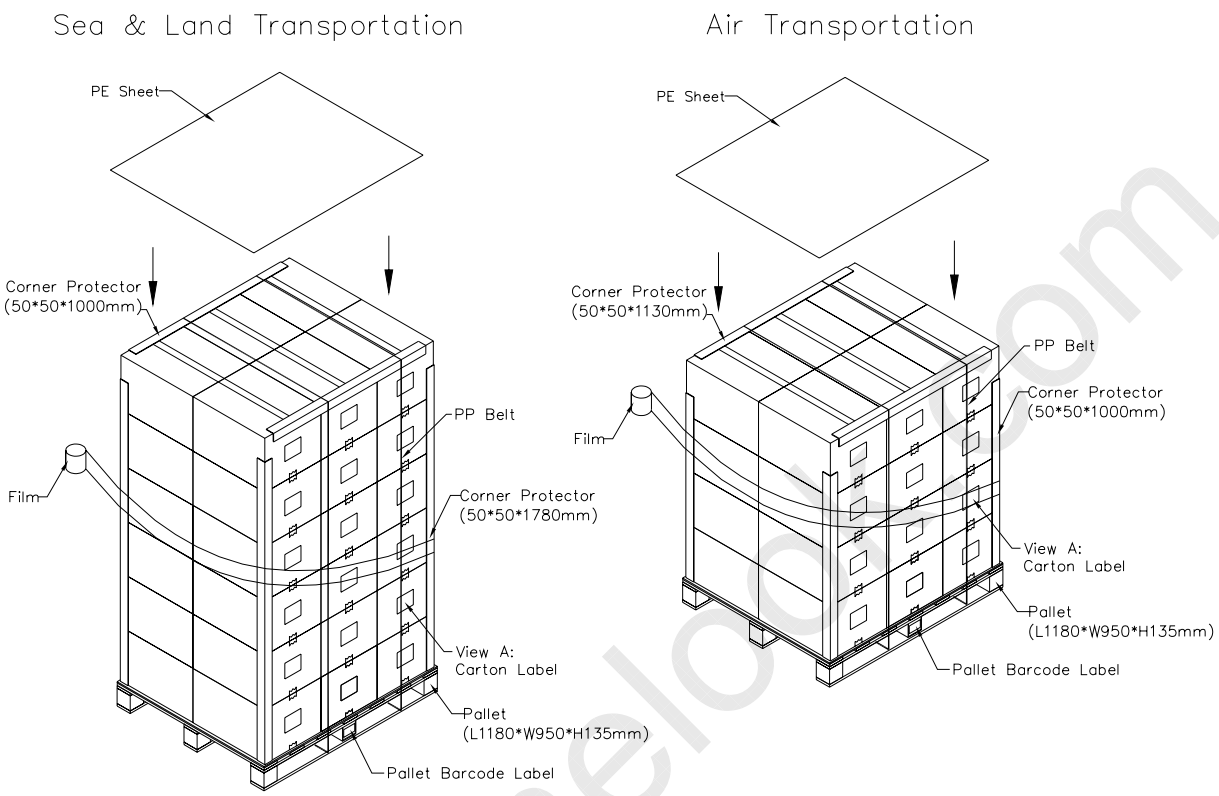

Figure. 9-2 Packing method

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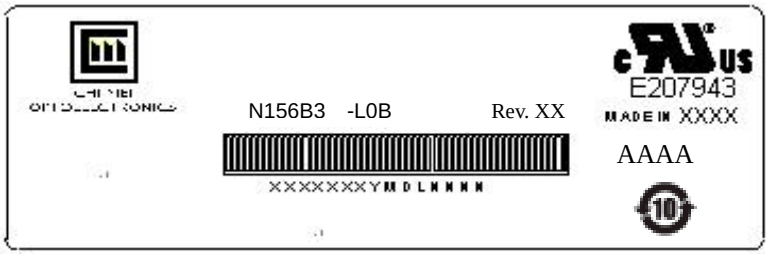
10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: N156B3 - L0B

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N

- Serial No.
- Product Line
- Year, Month, Date
- CMO Internal Use
- Revision
- CMO Internal Use

(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL logo: “AAAA” especially stands for panel manufactured by CMO China satisfying UL requirement. “LEOO” and “COCKN” is the CMO’s UL factory code for Ningbo factory..

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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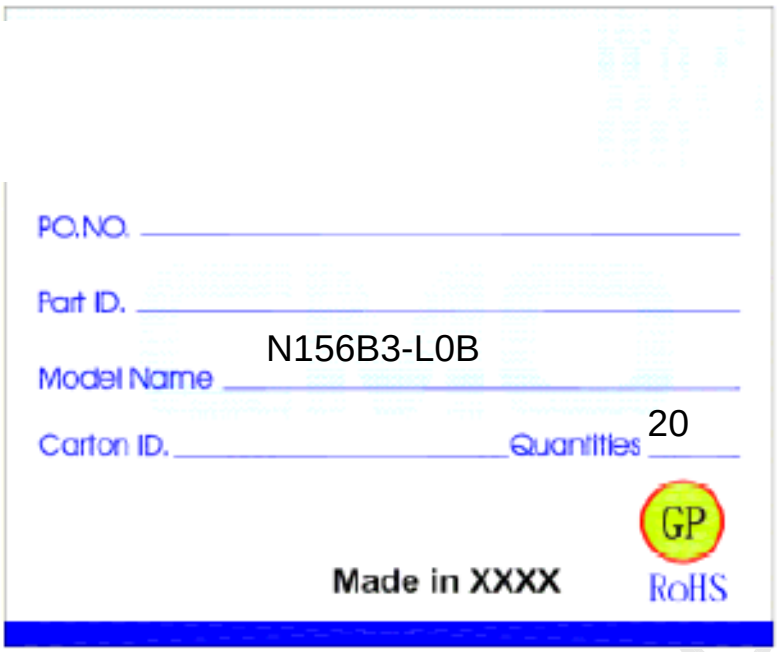
10.2 CARTON LABEL



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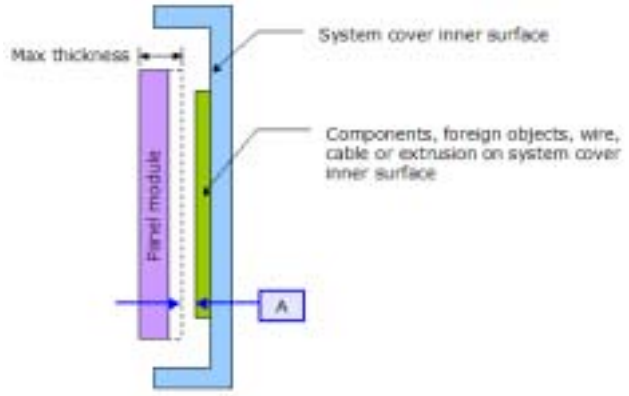
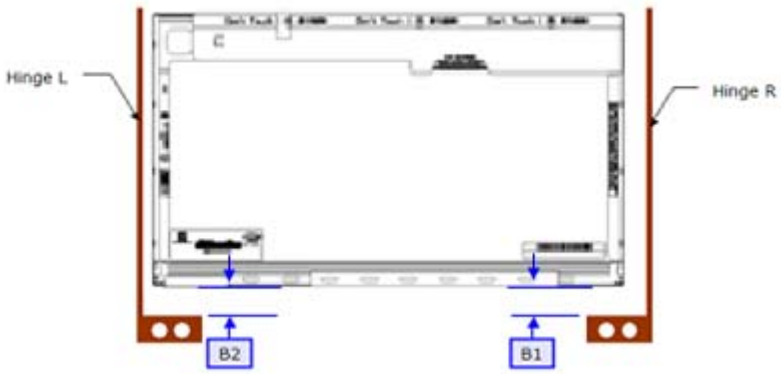
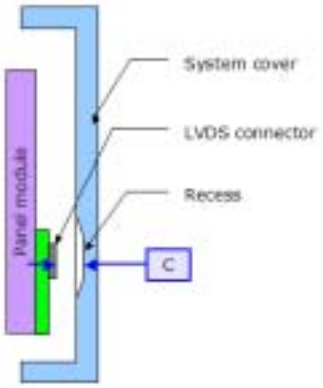
11.SYSTEM COVER DESIGN NOTICE

1.	**Design gap A between panel & any components on system cover**
	
Definition	a). Sufficient gap between panel & system is a must for preventing from backpack or pogo test fail. b). Zero gap from panel's maximum thickness boundary to any components, foreign objects, wire, cable or extrusion on system cover inner surface is forbidden.
2	**Design gap B1 & B2 between panel & protrusions**
	
Definition	2.0mm min. gap is recommended between panel & system cover for preventing from shock related failures
3	**Design gap C between LVDS connector & system cover inner surface**
	
Definition	a). Sufficient gap between LVDS connector & system cover inner surface is essential for preventing from pooling & white spot after backpack or pogo test. b). A partial recess by trimming off the cover surface is recommended for gaining extra gap between LVDS connector & system cover.

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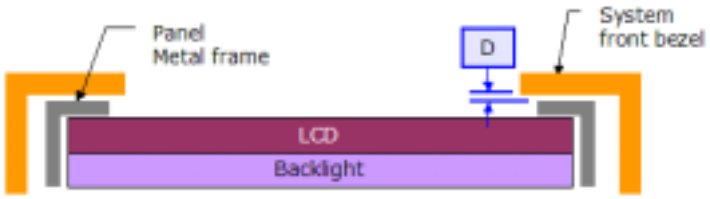
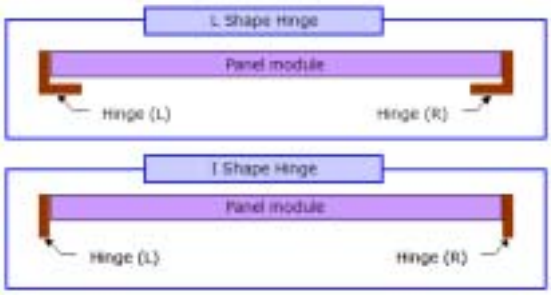
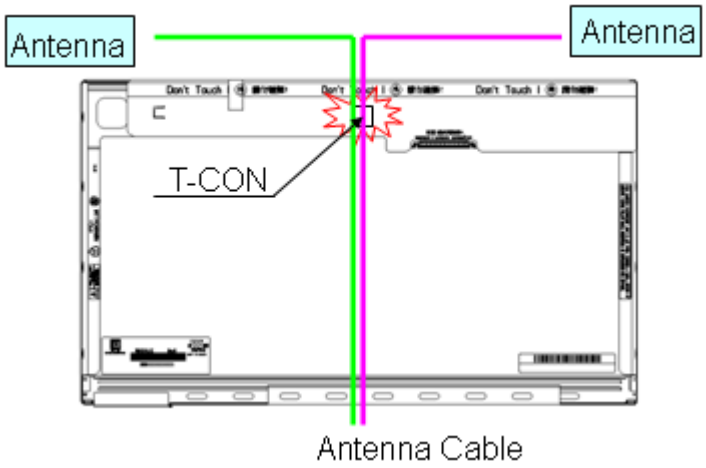
4	**Design gap D between system front bezel & panel metal frame**
	
Definition	a). Sufficient gap between system front bezel & panel metal frame is a must for preventing from pooling or glass broken. b). Zero gap or interference is forbidden.
5	**Hinge structure examination**
	
Definition	" L " shape hinge is recommended than " I " type for preventing shock test deformation of hinge & panel
6	**Interference examination (T-CON vs antenna cable and WebCam wire)**
	
Definition	a). Antenna cable or WebCam wire overlap with T-CON is forbidden for preventing from abnormal display, noise, pooling & white spot after backpack test, hinge test, twist test or pogo test. b). Antenna cable or WebCam wire bypass T-CON is recommended.

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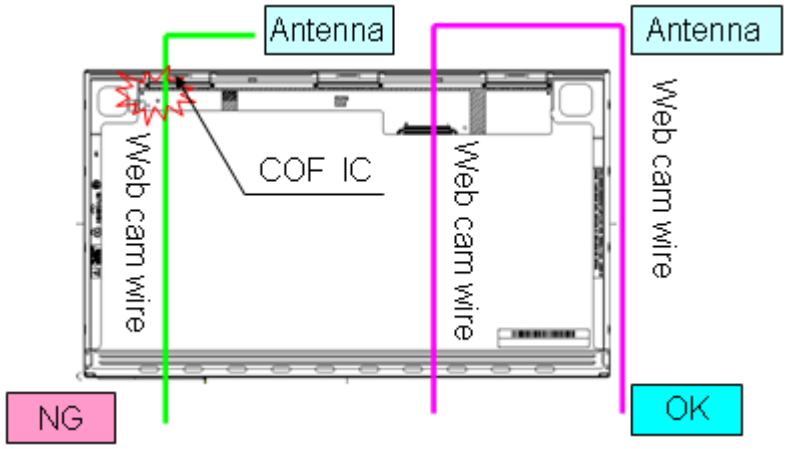
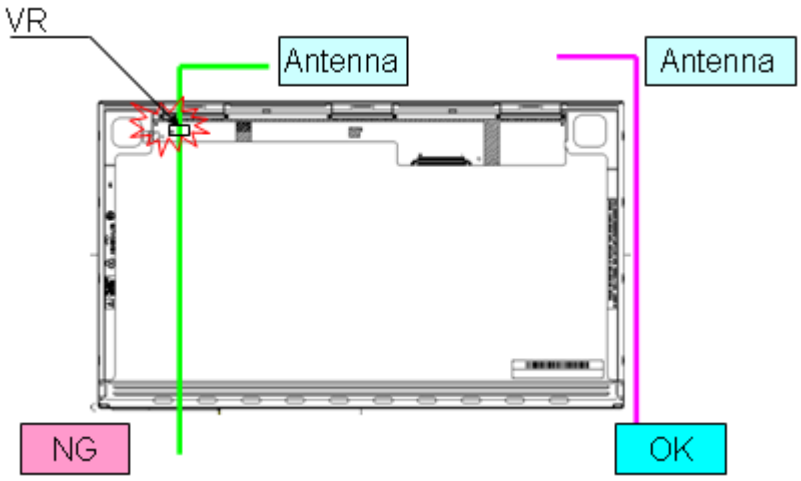
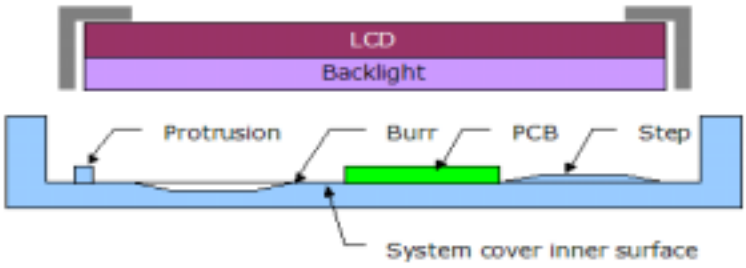
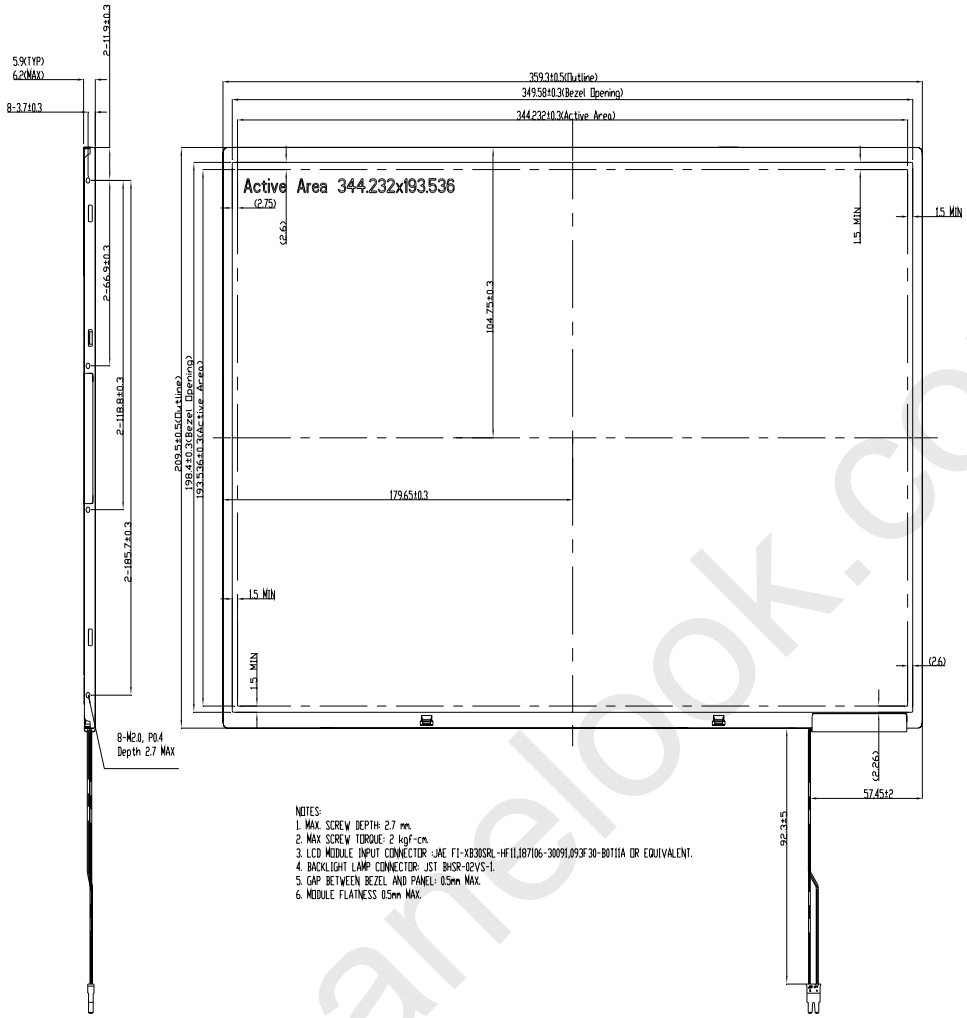
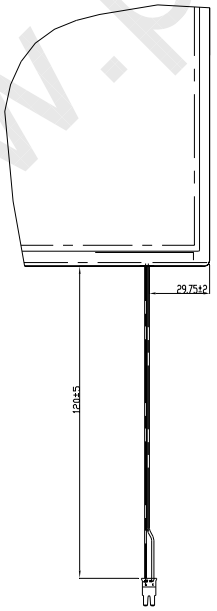
7	**Interference examination (COF IC vs antenna cable and WebCam wire)**
	
Definition	a). Antenna cable or WebCam wire overlap with COF especially COF IC is forbidden for preventing from IC crack, abnormal display after backpack test, hinge test, twist test or pogo test. b). Antenna cable or WebCam wire bypass COFs is recommended.
8	**Interference examination (VR vs antenna cable and WebCam wire)**
	
Definition	a). Antenna cable or WebCam wire overlap with VR is forbidden for preventing from abnormal display, pooling & white spot after backpack test, hinge test, twist test or pogo test. b). Antenna cable or WebCam wire bypass VR is recommended.
9	**System inner surface examination**
	
Definition	a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot or glass broken. b). Keeping flat surface underneath backlight is recommended.

Appendix. OUTLINE DRAWING





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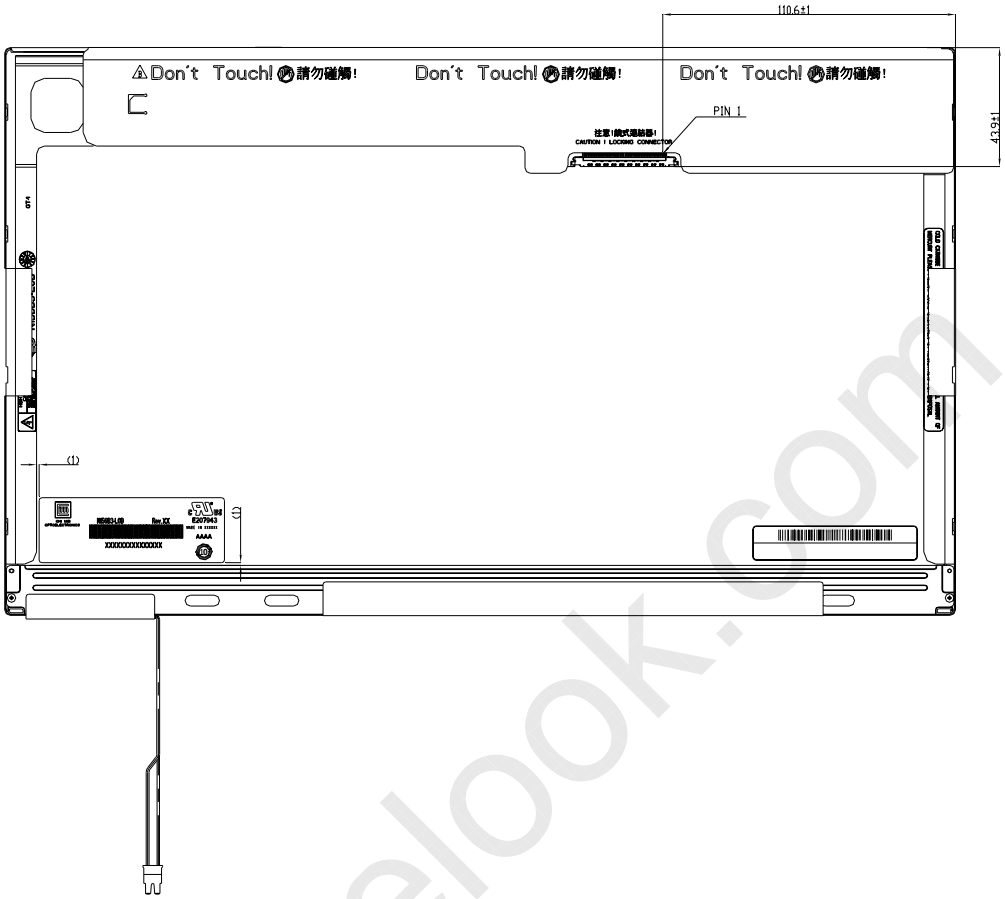
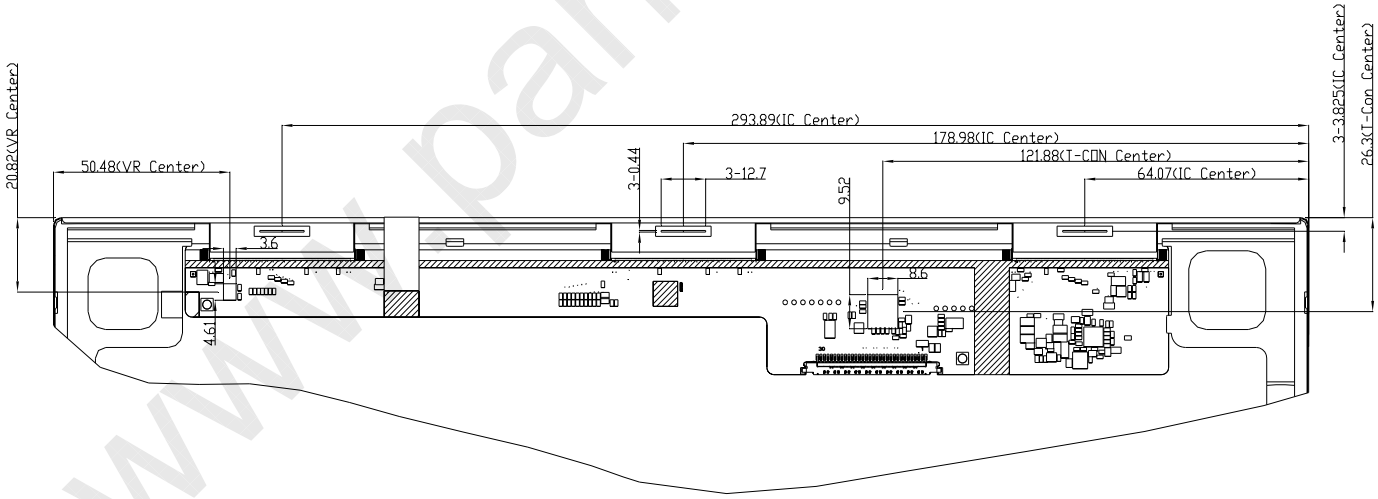
Model No.: N156B3-L0B

Approval





NOTES:
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAM OR OTHER FOREIGN OBJECTS OVER TCON AND VR LOCATION.